

<b>Notice of References Cited</b>	Application/Control No. 10/707,707		Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner Toniae M. Thomas		Art Unit 2822	Page 1 of 1

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	X	Wolf, Ph.D., Stanley, "Multilevel-Interconnect Technology for VLSI and ULSI," Silicon Processing for the VLSI Era - Vol. 2: Process Integration, Lattice Press, 1990, pp. 273.				

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.